Optimized Implementation of Encapsulation and Decapsulation of Classic McEliece on ARMv8

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Abstract. Recently, the results of the NIST PQC contest were announced. Classic McEliece, one of the 3rd round candidates, was selected as the fourth round candidate. Classic McEliece is the only code-based cipher in the NIST PQC finalists in third round and the algorithm is regarded as secure. However, it has low efficiency. In this paper, we propose an efficient software implementation of Classic McEliece, a code-based cipher, on 64-bit ARMv8 processors. Classic McEliece can be divided into Key Generation, Encapsulation, and Decapsulation. Among them, we propose an optimal implementation for Encapsulation and Decapsulation. Optimized Encapsulation implementation utilizes vector registers to perform 16-byte parallel operations, and optimize using the specificity of the identity matrix. Decapsulation implemented efficient Multiplication and Inversion on $\mathbb{F}_{2^m}$ field. Compared with the previous results, Encapsulation showed the performance improvement of up-to 1.99× than the-state-of-art works.

Keywords: 64-bit ARMv8 Processors, Code based Cipher, Classic McEliece, NIST PQC, Parallel implementation, KEM

1 Introduction

Classic McEliece is the only code-based cipher in the NIST PQC finalists. The basic structure is based on the McEliece [1] cryptosystem in 1978, and its stability has been verified through long-term research. In addition, the German Federal Office for Information Security recommends Classic McEliece as long-term security along with FrodoKEM [2].

Recently, NIST PQC final algorithms was decided. `CRYSTALS-KYBER`[3] was selected as public key encryption and key establishment algorithms. And as digital signature algorithms, `CRYSTALS`
`_DILITHIUM[4], FALCON[5], and SPHINCS+` [6] were selected. Optimal implementation research on ARMv8 for the selected algorithm is being actively conducted[7–12].

Although Classic McEliece is secure, it was not selected as a finalist due to the large size of the public key. However, NIST PQC is conducting the 4th candidate KEM, and it is judged that there is sufficient possibility because it is the only code-based cipher among candidate algorithms [13].

In this paper, we implement optimized Classic McEliece on ARMv8 processor. Our contributions are as follows:

1.1 Contribution

First Implementation of Classic McEliece on ARMv8 As far as we know, there is no Classic McEliece optimization implementation on ARMv8 yet. We present the first Classic McEliece optimization implementation of ARMv8.

Optimized Implementation of Encapsulation on ARMv8 We present optimized implementation of Encapsulation on ARMv8. Optimized the Encapsulation process by optimizing the computation when generating the syndrome. Most of the identity matrices in the syndrome generation process are zero, so we use the omitting possibility for optimization.

Optimized Implementation of Decapsulation on ARMv8 We present optimized implementation of Decapsulation on ARMv8. During decapsulation, Multiplication operations and Inversion operations are performed on extended binary finite-field $\mathbb{F}_{2^m}$, where m is 12 or 13. Multiplication operations and Inversion operations take a lot of time. Therefore, in this paper, Multiplication and Inversion operations on $\mathbb{F}_{2^m}$ operating in decapsulation are efficiently implemented using ARM instructions.

2 Preliminaries

2.1 Classic McEliece

Classic McEliece is designed to combine the advantages of McEliece and Niederreiter. The existing McEliece uses a Generator Matrix(G) for the public key, whereas Classic McEliece uses the Parity Check Matrix(H) used as the public key in Niederreiter. Classic McEliece is designed with a simple matrix multiplication process for Encapsulation and Decapsulation, allowing for fast computation. It also has the advantage of having a shorter Ciphertext compared to the existing Ciphertext. On the other hand, the length of the public key is very long and the key generation process takes a long time. The length of the public key is 256KB to 1.3MB, using it difficult to use on low-end devices with small memory space. Classic McEliece parameters are shown in Table 1.

Classic McEliece algorithm can be divided into three processes: a key generation process, an encryption process(Encapsulation), and a decryption process(Decapsulation).

- **Key Generation** In the Key Generation process, first, g(x) of degree t required for Goppa code generation and L called a support set are generated. Generate H(parity check matrix) using g(x) and L. The generated H is converted to binary form and converted to systematic form by performing

Gaussian elimination. That is, it is converted to the form H = $(I_{n-k}|T)$, and after removing I_{n-k}(Identity Matrix), the remaining **T** matrix is used as a public key. The private key consists of **g(x)** and **L**, which are used to generate the Goppa code, and a randomly generated **s**. In conclusion, the public key is **T** and the private keys are **g(x)**, **L**, and **s**.

- **Encapsulation** In the Encapsulation process, a random vector(e) with weight t is first generated. A syndrome(C_0) is generated using the generated e and the public key(T). It uses the value of e and the number 2 to generate a hash value(C_1 = Hash(2, e)) and combines the two values(C = $C_0|C_1$) to finally produce the ciphertext(C). Finally, for the session key, the hash value of the number 1, e, C will be the session key(K = Hash(1, e, C)).
- **Decapsulation** In the Decapsulation process, Decapsulation is performed using the delivered value of C and the owned private key. The value of e(error matrix) can be obtained by performing syndrome decoding with the syndrome(C_0) included in C(ciphertext) and the private key. It is determined whether there is an error by comparing the hash value with the number 2 in front of the e value obtained through syndrome decoding and the C_1 value included in the transmitted C(ciphertext). If the two values are the same, the hash value of the numbers 1, e, and C is computed to obtain the session key.

Table 1. Parameters of Classic McEliece; **m** is $log_2 q$ (q is the size of the field used); **n** is length of code, and **t** is the sizes of guaranteed error-correction capability;

Algorithm	m	n	t	security level	Public key	Secret key
Mceliece 348864	12	3,488	64	1	261,120	6,492
Mceliece 460896	13	4,608	96	3	524,160	13,608
Mceliece 6688128	13	6,688	128	5	1,044,992	13,932
Mceliece 6960119	13	6,960	119	5	1,047,319	13,948
Mceliece 8192128	13	8,192	128	5	1,357,824	14,120

2.2 ARMv8 Processor

ARM is an ISA(Instruction Set Architecture) high-performance embedded processor. ARMv8-A supports both 32-bit AArch32 and 64-bit AArch64 architectures for backward compatibility. ARMv8-A provides 31 64-bit general-purpose registers from $x0$ to $x30$ and 32 128-bit vector registers from $v0$ to $v31$. In this case, the general purpose registers can also be used as 32-bit registers from $w0$ to $w30$. Vector registers can be operated in parallel. The vector registers can be processed by dividing stored values into specific units. There are four types of units supported: byte (8-bit), half word (16-bit), single word (32-bit), and double word (64-bit). A vector instructions (called ASIMD or NEON) is used for the vector register to perform parallel operation. Table 2 shows that instruction lists for proposed implementations [14].

Table 2. Summarized instruction set of ARMv8 for Classic McEliece; `Xd, Vd`: destination register (general, vector), `Xn, Vn, Vm`: source register (general, vector, vector), `Vt`: transferred vector register.

asm	Operands	Description	Operation
ADD	Xd, Xn, Xm	Add	Xd ← Xn + Xm
AND	Xd, Xn, Xm(,shifted #amount)	Bitwise AND(shifted register)	Xd ← Xn & (Xm <<#amount or Xm >>#amount)
SUB	Xd, Xn, #imm	Substact (immediate)	Xd ← Xn - Xm
EOR	Xd, Xn, Xm	Bitwise Exclusive OR	Xd ← Xn ⊕ Xm
EOR	Xd, Xn, Xm(,shifted #amount)	Bitwise Exclusive OR (shift register)	Xd ← Xn ⊕ (Xm <<#amount or Xm >>#amount)
ORR	Xd, Xn, Xm(,shifted #amount)	Bitwise OR(shifted register)	Xd ← Xn | (Xm <<#amount or Xm >>#amount)
LD1	Vt.T, [Xn]	Load multiple single-element structures to one, two, three, or four registers	Vt ← [Xn]
LDR	Xt, [Xn], amount	Load Register	Xt ← [Xn]
MOV	Vd.T, Vn.T	Move(vector)	Vd ← Vn
MOV	Vd.Ts[index1], Vn.Ts[index2]	Move vector element to another vector element	Vd ← Vn
MOV	Xd, Xn	Move(register)	Xd ← Xn
MOV	Xd, #imm	Move(immediate)	Xd ← imm
RET	{Xn}	Return from subroutine	Return
LSL	Xd, Xn, #shift	Logical Shift Left(immediate)	Xd ← Xn <<#shift
LSR	Xd, Xn, #shift	Logical Shift Right(immediate)	Xd ← Xn >>#shift
MUL	Xd, Xn, Xm	Multiply	Xd ← Xn × Xm
BIC	Vd.T, Vn.T, Vm.T	Bitwise bit Clear(vector, register)	Clear
LDRB	Wt, [Xn], #amount	Load Register Byte	Wt ← [Xn]
LDRH	Wt, [Xn], #amount	Load Register Half word	Wt ← [Xn]
STRB	Wt, [Xn], #amount	Store Register Byte	Wt → [Xn]
STRH	Wt, [Xn], #amount	Store Register Half word	Wt → [Xn]
CBNZ	Wt, Label	Compare and Branch on Nonzero	Go to Label
CBZ	Wt, Label	Compare and Branch on Zero	Go to Label

2.3 Previous Implementations of Post Quantum Cryptography on ARM Processors

Becker et al. proposed implemented an optimization for Barrett multiplication using the 64-bit ARM Cortex-A NEON vector instruction [8]. They are the combination of Montgomery multiplication and Barrett reduction resulting in Barrett multiplication which allows particularly efficient modular one-known-factor multiplication using the NEON vector instructions. And proposed novel techniques combined with fast two-unknown-factor Montgomery multiplication, Barrett reduction sequences, and interleaved multi-stage butterflies result in significantly faster code. As a result, in the Saber, NTTs are far superior to Toom-Cook multiplication on the ARMv8-A architecture, outrunning the matrix-to-vector polynomial multiplication by 2.0×. On the Apple M1, the matrix-vector products run 2.1× and 1.9× faster for Kyber and Saber respectively.

Sanal et al. proposed implemented Kyber encryption on 64-bit ARM Cortex-A and Apple A12 processors [9]. They improved the performance of noise sampling, Number Theoretic Transform (NTT), and symmetric function implementations based on an AES accelerator. As the result, the proposed Kyber512 implementation on ARM64 improved the previous work by 1.72×, 1.88×, and 2.29× for key generation, encapsulation, and decapsulation, respectively. And, the proposed Kyber512-90s implementation(using AES accelerator) is improved by 8.57×, 6.94×, and 8.26× for key generation, encapsulation, and decapsulation, respectively.

Chen et al. proposed implemented Classic McEliece optimizations on the ARM Cortex-M4 [15]. The Cortex-M4 is a family of 32-bit ARMv7. Due to the small RAM size of 192KB, the public key was stored in the ROM and implemented. In addition, performance improvement was shown by using Quick sort when generating errors in the encapsulation process and applying the bitslicing technique for matrix multiplication optimization. Decapsulation was also optimized for bitslicing and Radix-16 implementation. As a result, compared to `FrodoKEM`, which has similar security strength, performance improvement was 79× faster in Encapsulation and 17× faster in Decapsulation.

3 Proposed Method

3.1 Optimized Implementation of Encapsulation

Excluding the hash process from encapsulation, it can be divided into two processes: random vector generation and syndrome generation. In this paper, we optimize the syndrome generation process. This process is called the ENCODE process. The encoding process adds an identity matrix to the public key T to create a parity check matrix. Then the parity check matrix is multiplied by a randomly generated e matrix. `ENCODE` is defined as follow:

$$\text{Define } H = (I_{n-k}|T).$$
$$\text{Compute and return } C_0 = He \in \mathbb{F}_2^{n-k}$$

Figure 1 shows the `ENCODE` process. 8 Rows are each matrix multiplied by the error and then combined into 1 S. At this time, it can be seen that 96-byte corresponding to the identity matrix are 0 except for 1-byte. Of course, most of the values of the error matrix are also 0, but it is impossible to know which index has a 0 value. That is, the operation of the identity matrix part except for the public key may be omitted except for 1-byte.

Algorithm 1 shows the implementation of the identity matrix part. For non-zero values, the eight values (1,2,4,8,16,32,64,128) are used repeatedly. This repeated value is **n** used in line 4. Since the error only needs to be computed for

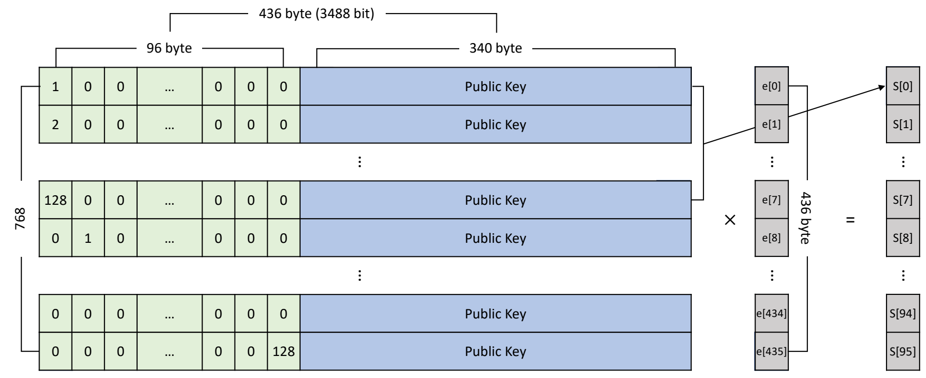

Fig. 1. `ENCODE` process of Encapsulation(In Classic McEliece-348864)

Algorithm 1 Assembly code implementing a macro that calculates only 1-byte of the identity matrix part(x3:error matrix address, x5:non-zero index in identity matrix, n:(1,2,4,8,16,32,64,128))

```
.macro row_front  n
 1: movi.16b v0, #0
 2: add x3, x2, x5
 3: ldrb w6, [x3]
 4: and w6, w6, #\n
 5: mov.b v0[0], w6
 6: add x3, x2, #96
.endm
```

Algorithm 2 Syndrome 1-bit value operation macro(n:(1,2,4,8,16,32,64,128), i: Bit index when storing as bytes in S, v0: (public key × error))

```
.macro calculate_s_1bit  n, i
 1: row_front \n
 2: row_process_21
 3: row_last

 4: mov.d v3[0], v0[1]
 5: eor.16b v0, v0, v3
 6: mov.s v3[0], v0[1]
 7: eor.16b v0, v0, v3
 8: mov.h v3[0], v0[1]
 9: eor.16b v0, v0, v3
10: mov.b v3[0], v0[1]
11: eor.16b v0, v0, v3
12: mov.s w9, v0[0]
13: and x9, x9, #0xff
14: lsr x10, x9, #4
15: eor x9, x9, x10
16: lsr x10, x9, #2
17: eor x9, x9, x10
18: lsr x10, x9, #1
19: eor x9, x9, x10
20: and x9, x9, #1
21: lsl x9, x9, #\i
22: orr x8, x8, x9
.endm
```

non-zero values, the operation is performed by calling only the error values that have an index equal to the non-zero matrix index. The index of the non-zero matrix is stored in the **x5** register used in line 3. This index is incremented by 1 after 8 iterations (1,2,4,8,16,32,64,128). **x3** is the address of the error matrix. It is computed by incrementing this value by **x5**(index) and then calling the value. Finally, correct the address of the error so that it is the same as the index where the public key value is stored.

In this paper, 16-byte parallel operation was performed using ARMv8 vector registers. Algorithm 2 is the assembly code to calculate the 1-bit syndrome. In lines 1-3, the public key and the error are computed in parallel and stored in the v0 register divided into 16 bytes. lines 4-11 collect the divided values into 1-byte. Finally, lines 12-22 perform an operation to obtain a 1-bit value from the calculated value. In line 21, i means the bit position in the byte. If this is repeated 8 times, one syndrome byte is calculated.

And in this paper, 8-byte parallel operation was performed using general registers. Algorithm 3 is an assembly code for calculating 1-bit syndrome using general registers, and has the similarly as Algorithm 2. In lines 1-3, the public key and the error are computed in parallel and stored in the **x6** register divided into 8-byte. lines 4-9 collect the divided values into 1-byte. Finally, lines 10-19 perform an operation to obtain a 1-bit value from the calculated value. In line 18, i is the same as i in Algorithm 2.

3.2 Optimized Implementation of Decapsulation

Decapsulation uses a decoder of the constant-time Berlekamp-Massey (BM) algorithm. Inside the BM algorithm, Multiplication and Inversion are performed on the extended binary finite-filed $\mathbb{F}_{2^m}$. The expensive operations on public keys are multiplication and inversion on finite-field. Therefore, in this paper, optimization of multiplication and inversion on $\mathbb{F}_{2^m}$ used in decapsulation is performed

Algorithm 3 Syndrome 1-bit value operation macro using only general registers (n:(1,2,4,8,16,32,64,128), i: Bit index when storing as bytes in S, x6: (public key × error))

```
.macro calculate_s_1bit_g n, i
row_front \n
row_process_21
row_last

lsr x7, x6, #32
eor x6, x6, x7
lsr x7, x6, #16
eor x6, x6, x7
lsr x7, x6, #8
eor x9, x6, x7
and x9, x9, #0xff
lsr x10, x9, #4
eor x9, x9, x10
lsr x10, x9, #2
eor x9, x9, x10
lsr x10, x9, #1
eor x9, x9, x10
and x9, x9, #1
lsl x9, x9, #\i
orr x8, x8, x9
.endm
```

(m is 12 or 13). In the specification, $\mathbb{F}_{2^{12}}$ consists of $\mathbb{F}_2[x]/(x^{12}+x^3+1)$ and $\mathbb{F}_{2^{13}}$ consists of $\mathbb{F}_2[x]/(x^{13}+x^4+x^3+x+1)$ [15].

Multiplication on $\mathbb{F}_{2^{13}}$. Multiplication on $\mathbb{F}_{2^m}$ proceeds as follows. Multiplication is performed on two m-bit values. At this time, since the multiplication result may be out of the range of $\mathbb{F}_{2^m}$, the multiplication is completed on $\mathbb{F}_{2^m}$ by performing modular reduction on the multiplication result value.

Algorithm 4 is an optimization implementation code for multiplication on $\mathbb{F}_{2^{13}}$. As shown in Table 2, ARMv8 general-purpose registers can implement logical operations and shift operations using one instruction. The part corresponding to lines 4-11 of Algorithm 4 implements the Multiplication part. The omitted part proceeds as follows. As shown in line 6, the SHIFT operation is performed by 1 to the left and the AND operation is performed. This SHIFT operation is a process of increasing the value by 1 up to $m-1$ and performing the operations from lines 6 to 8 in the same way. Finally, it can be seen that the $m-1$ value of 12 is applied in line 9. And if multiplication is finished through this process, there may be a result of multiplication out of $\mathbb{F}_{2^{13}}$. Therefore, after performing modular reduction, the operation corresponding to lines 12 to 24, on the result of multiplication, the result of the operation is returned. As such, it was possible to efficiently implement the corresponding part according to the characteristics of the ARM instructions.

Algorithm 5 is an optimization implementation code for multiplication on $\mathbb{F}_{2^{13t}}$. t corresponds to the value of t in Table 1. **w7** is the index value of loop0. **w8** and **w9** is the index value of loop1 and loop2. **w12** is the index value of loop3. In the lines 18, 39, 44, 49,and 54, Multiplication on $\mathbb{F}_{2^{13}}$, the operation of Algorithm 4, is performed. For the lines 6-12, after the operation, the operation to initialize to 0 is performed for the corresponding array in which the operation result value is to be stored. The lines 13-33 perform a multiplication operation

Algorithm 4 Multiplication on $\mathbb{F}_{2^{13}}$($x0$, $x1$ is input register; $x13$, $x14$ is temporary registers).

```
Input: a ($\mathbb{F}_{2^{13}}$), b ($\mathbb{F}_{2^{13}}$)
Output: a * b ($\mathbb{F}_{2^{13}}$)

 1: mov x10, x0
 2: mov x20, x1
 3: mov x3, #1

 4: and x14, x20, x3, lsl #1
 5: mul x13, x10, x14

 6: and x14, x20, x3, lsl #2
 7: mul x14, x10, x14
 8: eor x13, x13, x14
    ⋮
 9: and x14, x20, x3, lsl #12
10: mul x14, x10, x14
11: eor x13, x13, x14

12: and x14, x13, #0x1FF0000
13: eor x13, x13, x14, lsr #9
14: eor x13, x13, x14, lsr #10
15: eor x13, x13, x14, lsr #12
16: eor x13, x13, x14, lsr #13

17: and x14, x13, #0x000E000
18: eor x13, x13, x14, lsr #9
19: eor x13, x13, x14, lsr #10
20: eor x13, x13, x14, lsr #12
21: eor x13, x13, x14, lsr #13

22: lsl x14, x3, #13
23: sub x14, x14, #1
24: and x0, x13, x14
```

on the two input values. The lines 35-65 performs the reduction operation on the results of the lines 13-33.

Inversion on $\mathbb{F}_{2^{13}}$. Inversion operation on $\mathbb{F}_{2^{13}}$ can obtain by dividing 1($\mathbb{F}_{2^{13}}$) input value. Algorithm 6 represents the $(\mathbf{S}^2)^2$ operation on the input value as part of the inversion operation(in this case, the input value is referred to as $\mathbf{S}(\mathbb{F}_{2^{13}})$. Operation on the square of the input value $\mathbf{S}$ can be calculated by changing the OR operation, SHIFT operation, and AND operation. This can be implemented as lines 3-10 of Algorithm 6. The OR operation, which is one of the logical operations, was also efficiently implemented so that the OR operation proceeds after the SHIFT operation with one ORR instruction in the same way as the AND instruction. And, as in multiplication on $\mathbb{F}_{2^m}$, the result obtained after the operation may be out of the range of $\mathbb{F}_{2^{13}}$, so the operation is completed by performing modular reduction on the result value.

4 Evaluation

Implementations were evaluated on a MacBook Pro 13 with the Apple M1 chip that can be clocked up to 3.2 GHz. Since ARMv8 does not have a Classic McEliece implementation, the performance is compared with the existing PQClean project reference code [16].

Encapsulation(up to `ENCODE`) was implemented in two ways. The two methods are parallel operation using vector register and parallel operation using general register, respectively. Therefore, we measured the operation time(”up to”

Algorithm 5 Multiplication on $\mathbb{F}_{2^{13t}}$(In Classic McEliece-460896)($x0$, $x1$, $x2$ is input register; $w8, w9, w11, w12$ is index.

```
Input: a ($\mathbb{F}_{2^{13t}}$), b ($\mathbb{F}_{2^{13t}}$)
Output: a * b ($\mathbb{F}_{2^{13t}}$)
 1: mov $x3$, #1
 2: mov $w8$, #$t$
 3: mov $w9$, #$t$
 4: mov $w12$, #$t-1$
 5: mov $w11$, #$t*2$

 6: loop0:
 7:   mov $w23$, #0
 8:   strh $w23$, [$x0$], #2
 9:   add $w11$, $w11$, #$-2$
10:   cbnz $w11$, loop0
11:   add $x0$, $x0$, #$-t*2*2$
12:   ldrh $w7$, [$x1$]

13: loop1:
14:   ldrh $w15$, [$x2$]
15:   ldrh $w23$, [$x0$]
16:   mov $w10$, $w7$
17:   mov $w6$, $w15$
18:   gf_mul
19:   eor $w23$, $w23$, $w13$
20:   add $x2$, $x2$, #2
21:   strh $w23$, [$x0$], #2
22:   add $w8$, $w8$, #$-1$
23:   cbnz $w8$, loop1
24:   cbz $w8$, loop2

25: loop2:
26:   add $x1$, $x1$, #2
27:   ldrh $w7$, [$x1$]
28:   add $x0$, $x0$, #$-(t*2)-2$
29:   add $x2$, $x2$, #$-t*2$
30:   mov $w8$, #$t$
31:   add $w9$, $w9$, #$-1$
32:   cbnz $w9$, loop1
33:   cbz $w9$, loop3

34: loop3:
35:   add $x0$, $x0$, #188
36:   ldrh $w23$, [$x0$]
37:   mov $x10$, $x23$
38:   mov $x6$, #714
39:   gf_mul
40:   mov $x24$, $x13$

41:   ldrh $w23$, [$x0$]
42:   mov $x10$, $x23$
43:   mov $x6$, #5296
44:   gf_mul
45:   mov $x25$, $x13$

46:   ldrh $w23$, [$x0$]
47:   mov $x10$, $x23$
48:   mov $x6$, #728
49:   gf_mul
50:   mov $x26$, $x13$

51:   ldrh $w23$, [$x0$]
52:   mov $x10$, $x23$
53:   mov $x6$, #5881
54:   gf_mul
55:   mov $x5$, $x13$

56:   add $x0$, $x0$, #$-170$

57:   ldrh $w23$, [$x0$]
58:   eor $w23$, $w23$, $w24$
59:   strh $w23$, [$x0$], #$-12$
60:   ldrh $w23$, [$x0$]
61:   eor $w23$, $w23$, $w25$
62:   strh $w23$, [$x0$], #$-2$
63:   ldrh $w23$, [$x0$]
64:   eor $w23$, $w23$, $w26$
65:   strh $w23$, [$x0$], #$-8$
66:   ldrh $w23$, [$x0$]
67:   eor $w23$, $w23$, $w5$
68:   strh $w23$, [$x0$], #2
69:   add $w12$, $w12$, #$-1$
70:   cbnz $w12$, loop3
```

Algorithm 6 Partial operation process of inversion operation on $\mathbb{F}_{2^{13}}$($x0$ is input register; $x11$, $x13$, $x14$ is temporary registers).

Input: a($\mathbb{F}_{2^{13}}$)
Output: $(a^2)^2(F_{2^{13}})$

```
 1: mov x10, x0
 2: mov x12, #1

 3: orr x11, x10, x10, lsl #24
 4: and x10, x11, #0x000000FF000000FF
 5: orr x11, x10, x10, lsl #12
 6: and x10, x11, #0x000F000F000F000F
 7: orr x11, x10, x10, lsl #6
 8: and x10, x11, #0x0303030303030303
 9: orr x11, x10, x10, lsl #3
10: and x10, x11, #0x1111111111111111

11: and x13, x10, #0x0001FF0000000000
12: eor x10, x10, x13, lsr #9
13: eor x10, x10, x13, lsr #10
14: eor x10, x10, x13, lsr #12
15: eor x10, x10, x13, lsr #13
16: and x13, x10, #0x000000FF80000000
17: eor x10, x10, x13, lsr #9
18: eor x10, x10, x13, lsr #10
19: eor x10, x10, x13, lsr #12
20: eor x10, x10, x13, lsr #13

21: and x13, x10, #0x000000007FC00000
22: eor x10, x10, x13, lsr #9
23: eor x10, x10, x13, lsr #10
24: eor x10, x10, x13, lsr #12
25: eor x10, x10, x13, lsr #13

26: and x13, x10, #0x00000000003FE000
27: eor x10, x10, x13, lsr #9
28: eor x10, x10, x13, lsr #10
29: eor x10, x10, x13, lsr #12
30: eor x10, x10, x13, lsr #13

31: lsl x14, x3, #13
32: sub x14, x14, #1
33: and x0, x13, x14
```

Table 3. Encapsulation (up to `ENCODE`) Evaluation result on ARMv8 processors(Apple M1) in terms of execution timing(i.e. clock cycles) and compile option `-O3`.(v is vector register and g is general register.)

Algorithm	mceliece 348864	mceliece 460896	mceliece 6688128	mceliece 8192128
[16]	7,426.531	10,177.125	21,789.469	28,130.500
Our work(v)	3,741.219	7808.875	14,393.469	27,208.156
Our work(g)	6,502.188	13,337.344	25,058.688	29,757.313

means until the hashing process is performed) by repeating the two methods of encapsulation 10,000 times and compiled using the compile option `-O3` (i.e. fastest). Performance evaluation is given in Table 3.

It was confirmed that Encapsulation of our implementation using vector registers performed average 1.7× times higher than Encapsulation of our implementation using general registers.

The performance of the implementation of Encapsulation optimization using vector registers performed in Classic Mceliece 348864 is 1.99× times higher than [16]. The performance of the implementation of Encapsulation optimization using vector registers performed in Classic Mceliece 460896 is 1.30× times higher than [16]. The performance of the implementation of Encapsulation optimization using vector registers performed in Classic Mceliece 6688128 is 1.51× times higher than [16]. The performance of the implementation of Encapsulation optimization using vector registers performed in Classic Mceliece 8192128 is 1.03× times higher than [16].

5 Conclusion

In this paper, we implemented the optimization of Classic McEliece Encapsulation and Decapsulation on ARMv8. Our Encapsulation implementation provides two methods. The two methods are 16-byte parallel operation using vector registers and 8-byte parallel operation using general registers. As a result of comparing the two methods, it was confirmed that the parallel operation using the vector register improved performance 1.7× compared to the parallel operation using the general register. As a result, our Encapsulation implementation achieves sufficient performance improvement was achieved only through syndrome-generation optimizations and efficiently performs 16-byte parallel operations using vector registers. Our Decapsulation uses ARM instruction efficiently to achieve sufficient performance improvement through optimization of multiplication and inversion operations for $\mathbb{F}_{2^m}$. As a result, Encapsulation showed a performance improvement of 1.03× ∼ 1.99×. As a future study, we propose an optimized implementation using Classic Mceliece on a low-end processor (i.e. AVR, RISC-V) and another optimized implementation of post-quantum cryptography on an ARMv8 processor.

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